Status CPLD Release Note

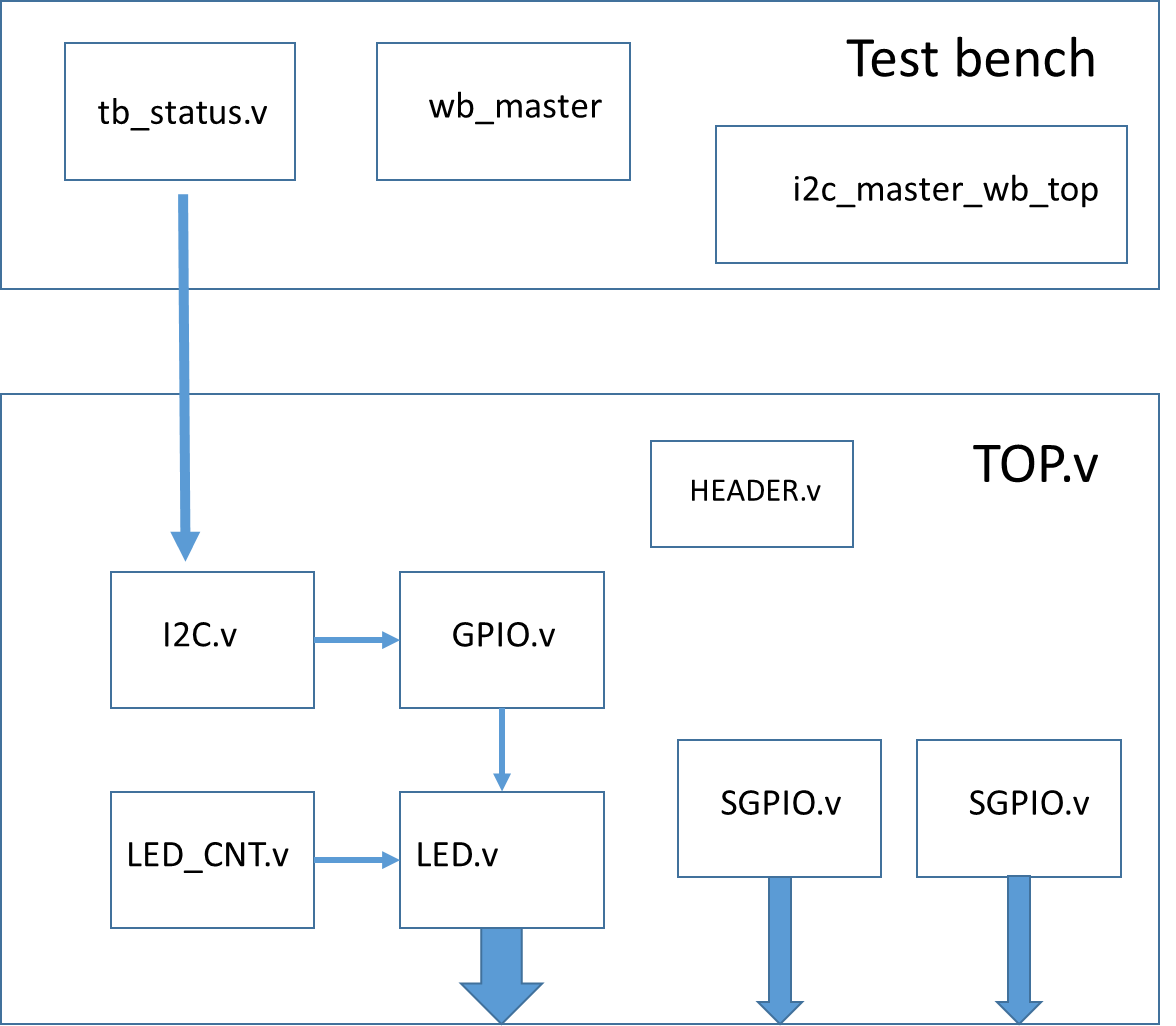
1. Folder Structure

SRC --- source code, including Verilog file and Constraint file.

SIM --- simulation code, including testbench and do file.

BLD --- project file

1. Code Structure



1. Simulation

tb\_status.v is the simulation top file, you can change the test flow in this module. There are five task in testbench including SGPIO, HEADER\_TEST, LED\_TEST, wb\_write and wb\_read.

About do file, there are two do file including tb\_status.do and status\_wave.do. The tb\_status.do is for compile and the status\_wave.do is only for waveform.

1. Project Build

All the project file is located in BLD folder, and the Status.ldf is for diamond.